**IN THE SPECIFICATION**

From page 15, line 20, amend the following paragraph as marked:

The culled packets selected by the recoder circuits have the headers stripped and the payload data in the packets is then decompressed and recompressed if necessary to reduce the bandwidth. This process is done by the recoding circuits 53, 55 and 57. These circuits receive the compressed or uncompressed data packets (or a combination of the two) on input lines 59, 61, 63 etc. and available bandwidth information from the management process 23 on bus 65 from the motherboard 27. ~~Sseparate~~ Separate buses are shown coupling the motherboard to multiple circuits, but in reality, all these buses may be simply the motherboard host bus and the data described herein just sent to each circuit when that circuit is addressed by the address lines on the bus. The available bandwidth information on bus 65 tells the recoding circuits how much additional compression to perform or that sufficient bandwidth is available on the downstream to meet the current bandwidth consumption in some embodiments. In the preferred embodiment, the available bandwidth information on bus 65 just tells the recoder circuits how much bandwidth is available on the downstream. In such embodiments, the recoder circuits decide for themselves how much bandwidth is consumed by the input streams and how much compression to perform to meet the bandwidth restrictions apparent from the information on bus 65. The recoding circuits are known and commercially available from Terayon Communications Systems, Inc. in Santa Clara, California. They were orginally designed by Imedia Corporation and are described in U.S. patents 5,956,088 and 5,877,812 and 5,862,140 all of which are hereby incorporated by reference.

A1 cont'd

From page 33, line 29, please amend the following paragraph as marked:

Gateway 308 also include circuitry to interface the LAN 246 at the customer premises #2 to several other sources of incoming programming and/or data and to send data out on upstream mediums other than the DSL line such as the PSTN or a satellite uplink or an HFC connection to a CATV headend. The details of the gateway 308 are given in the patent application HOME NETWORK FORORDERINGANDDELIVERYOFVIDEOONDEMAND,TELEPHONEANDOTHER DIGITAL SERVICES, filed 1/14/2000, serial number 09/483,681 which is hereby incorporated by reference, but some of the circuitry will be summarized here for completeness. For example, the gateway couples a CATV headend 314 and HFC data path 316 to LAN 246 via a cable modem 318 and various other circuits in the gateway that perform necessary services and routing of data to and from the LAN 246. The gateway includes tuner, A/D, decoder, demultiplexer and demodulation circuitry represented by block 320 which performs various functions to interface the gateway to HFC 316. The HFC 316 can carry downstream conventional FDMA analog video broadcasts for video conferencing or CATV delivery, digital video broadcasts and/or downstream ~~downstredam~~ DOCSIS data modulated onto upstream and downstream carriers. Thus, the gateway 308 can also request video-on-demand, video conferencing, wideband internet access or other services via the upstream logical channel on the HFC 316 as an alternative to DSL delivery.

A2 cont'd